**COMSATS INSTITUTE OF INFORMATION TECHNOLOGY ISLAMABAD ATTOCK CAMPUS**



**PROJECT REPORT DLD**

**2ND SEMESTER**

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| **Group Members** | **Registration numbers** |
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**Title:**

**BCD RIPPLE COUNTER**

1. **OBJECTIVES**

* It performs the operation of resetting automatically when there is a new clock input signal.
* The BCD code is wasteful as many of the 4-bit states (10-to-16) are not used but decimal displays have important applications.

1. **INTRODUCTION**

* Ripple counter is a special type of **Asynchronous** counter in which the clock pulse ripples through the circuit. The n-MOD ripple counter forms by combining n number of flip-flops. The n-MOD ripple counter can count 2n states, and then the counter resets to its initial value.
* Binary coded decimal (BCD) is a system of writing numerals that assigns a four-digit binary code to each digit 0 through 9 in a decimal (base-10) numeral. The four-bit BCD code for any particular single base-10 digit is its representation in binary notation.
* A binary coded decimal (BCD) is a serial digital counter that counts ten digits. And it resets for every new clock input. As it can go through 10 unique combinations of output, it is also called as “Decade counter”.
* A counter is basically used to count the number of clock pulses applied to a flip-flop. It can also be used for Frequency divider, time measurement, frequency measurement, distance measurement and also for generating square waveforms.
* Asynchronous counters are sometimes called ripple counters because the data appears to “ripple” from the output of one flip-flop to the input of the next. They can be implemented using “divide-by-n” counter circuits. Truncated counters can produce any modulus number count.
* Following are some important features of ripple counter:
* Different types of flip flops with different clock pulse are used.
* It is an example of an asynchronous counter.
* The flip flops are used in toggle mode.
* The external clock pulse is applied to only one flip flop. The output of this flip flop is treated as a clock pulse for the next flip flop.

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1. **REQUIRED COMPONENTS**

* D-Flip flop ICs
* Bread Board
* Connecting Wires
* Regulator IC
* Decoder
* 7 Segment Display
* Capacitors of 10µF AND 0.015µF
* Resistors

1. **CIRCUIT DIAGRAM ON PROTEUS**

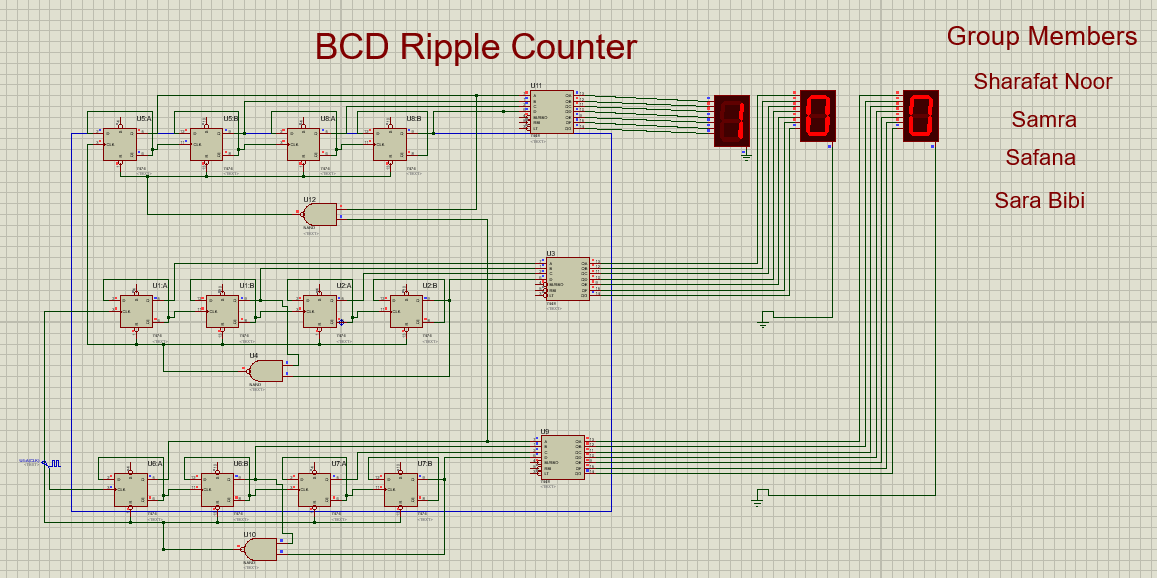
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Figure 1:Circuit diagram on proteus

1. **TRUTH TABLE**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Present State**  **(Q3 Q2 Q1 Q0)** | **Next State**  **(Q3+ Q2+ Q1+ Q0+)** | **D3** | **D2** | **D1** | **D0** |
| 0000 | 0001 | 0 | 0 | 0 | 1 |
| 0001 | 0010 | 0 | 0 | 1 | 0 |
| 0010 | 0011 | 0 | 0 | 1 | 1 |
| 0011 | 0100 | 0 | 1 | 0 | 0 |
| 0100 | 0101 | 0 | 1 | 0 | 1 |
| 0101 | 0110 | 0 | 1 | 1 | 0 |
| 0110 | 0111 | 0 | 1 | 1 | 1 |
| 0111 | 1000 | 1 | 0 | 0 | 0 |
| 1000 | 1001 | 1 | 0 | 0 | 1 |
| 1001 | 1010 | 1 | 0 | 1 | 0 |
| 1010 | 1011 | 1 | 0 | 1 | 1 |
| 1011 | 1100 | 1 | 1 | 0 | 0 |
| 1100 | 1101 | 1 | 1 | 0 | 1 |
| 1101 | 1110 | 1 | 1 | 1 | 0 |
| 1110 | 1111 | 1 | 1 | 1 | 1 |
| 1111 | 0000 | 0 | 0 | 0 | 0 |

Figure 2: General truth table for four D-flip flops

1. **ADVANTAGES**

* It can be easily designed by D-flip flop or T-flip flop.
* It can be used in low-speed circuits.
* It is used as Divide by-n counters.

1. **DISADVANTAGES**

* For Re synchronization, extra flip flop is needed.
* Additional feedback logic is needed to count the sequence of truncated counters (keep in mind that mod is not equal to 2n).
* The propagation delay of asynchronous counters is very large, while counting large number of bits.
* Due to propagation delay, counting errors may occur for high clock frequencies.
* They are slower as compared to synchronous counters.

1. **APPLICATIONS**

* They are used as frequency dividers, as divide by “N” counters.
* They are used for low noise emission and low power applications
* They are used in designing asynchronous decade counter.
* These counters are frequently used for measurement of Time, Measurement of Frequency, Measurement of Distance, Measurement of Speed, Waveform generation, Frequency Division, Digital Computers, Direct Counting etc.

1. **CONCLUSION**

BCD counters follow a sequence of ten states and count using BCD numbers from 0000 to 1001 and then returns to 0000 and repeats. Such a counter must have at least four flip-flops to represent each decimal digit, since a decimal digit is represented by a binary code with at least four bits giving a MOD-10 count.

Display decoder circuits can be constructed from combinational logic elements and there are many dedicated integrated circuits on the market to perform this function such as the 74LS47 BCD to 7-segment decoder/driver IC.

Most 7-segment displays are usually used in multi-digit counting applications so by cascading together more BCD counters, 4-digit counters giving displays with a maximum reading of 9999 can be constructed.

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